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TITLE: SEMICONDUCTOR DEVICE

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US-CL-CURRENT: 257/723,257/777 ,257/778

ABSTRACT:

PURPOSE: To realize highly reliable high density mounting on a wiring board by employing multistage or laminar flip-chip mounting of semiconductor chips.

CONSTITUTION: A first semiconductor chip 5a having a first bump electrode 6a is placed on a bonding pad 8a. A second semiconductor chip 5b having a second bump electrode 6b and flip-chip mounting the first semiconductor chip 5a while opposing active element regions 7a, 7b forming faces each other on the surface thereof is placed on a bonding pad 8b. Furthermore, a third semiconductor chip 5c having a third bump electrode 6c and flip-chip mounting the second

semiconductor chip 5b while opposing active element regions 7b, 7c forming
faces each other on the surface thereof is placed on a bonding pad 8c. The
semiconductor device is constituted in multilayer of three or more layers.
This constitution reduces wiring board area required for mounting greatly as
compared with the overall planar area of the semiconductor chips 5a-5c.

## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the semiconductor device which was applied to the semiconductor device, especially constituted mounting to a wiring substrate side for two or more semiconductor chips possible with high density.
[0002]
[Description of the Prior Art] The demand which a semiconductor device (a semiconductor chip or semiconductor device) has towards high integration in recent years, and mounts this kind of semiconductor device to a wiring substrate with high density is also increasing. And as a means to mount a semiconductor device with high density to a wiring substrate side, although various methods are also proposed, the flip chip mounting method is mainly performed recently. Flip chip mounting is wire bonding mounting. As compared with TAB mounting, it is because a semiconductor chip can be mounted with high density. Namely, wire bonding mounting The area which the lead pulled out from a semiconductor chip occupies by TAB mounting when a semiconductor chip is mounted is a semiconductor chip. One 2 to 3 times the area of this is needed. On the other hand, in FURIBBU chip mounting, the area of a semiconductor chip is sufficient for the component-side product of a semiconductor chip, and it can mount a semiconductor chip by the upper part of the body which adjoined mutually. Therefore, as compared with flip chip mounting, it is wire bonding mounting. The component-side product of a semiconductor chip TAB mounting It becomes about 1 / two to 1/3, and the limitation of densification is made.
[0003] By the way, since the aforementioned flip chip mounting is the so-called flat-surface mounting, packaging density also receives restrictions from a wiring substrate side, and there is a limitation also in the densification of mounting. such a problem -- receiving -- for example, -- as [ indicate / by IMC 90 Proceeding ] -- the laminating of the tape career of TAB mounting is carried out, and a means to arrange a semiconductor chip in lengthwise and to mount it in three dimensions is proposed as indicated by a means to mount a semiconductor chip in three dimensions, or EP&P 1990p76
[0004]
[Problem(s) to be Solved by the Invention] However, in the aforementioned 3-dimensional (target) mounting, when the size of the semiconductor chip mounted like **, for example, a memory chip, is not the same or a configuration is uneven, there is a problem that densification of mounting in alignment with the purpose cannot be attained.
[0005] The composition which, on the other hand, mounts the semiconductor chip from which size differs in multi-stage as shown in drawing 6 in cross section is also tried. That is, about each semiconductor chips 1a, 1b, and 1c from which size differs, wiring was extended from the bonding pad of an active element field side to the rear-face side, respectively, the 2nd bonding pad 2a, 2b, and 2c was formed in the rear face, and the composition which mounted each semiconductor chips 1a, 1b, and 1c in the 3rd page of a wiring substrate in multi-stage is taken through these 2nd bonding pads 2a, 2b, and 2c. however -- ****** it is difficult to form the 2nd bonding pad 2a, 2b, and 2c in the rear face of semiconductor chips 1a, 1b, and 1c, and it drills a hole in semiconductor chips 1a, 1b, and 1c and forms the 2nd bonding pad 2a, 2b, and 2c in this composition using this hole -- the above -- the drilling process of a hole is required Anyway, in composition of having illustrated to this drawing 6 , there are problems, such as becoming a cost rise.
[0006] Furthermore, as the semiconductor chip from which size differs is shown in drawing 7 in cross section, a laminating and the composition to arrange are also tried in multi-stage. That is, the composition which connected between mutual electrically by the wire bonding 4, and mounted each semiconductor chips 1a, 1b, and 1c from which size differs while mounting it on the 3rd page of a necessary wiring substrate in laminating one by one, having used the active element field side as the upper surface is taken. However, in this composition, since other semiconductor chips are mounted on the active element field side which makes the exoergic side of semiconductor chips 1a, 1b, and 1c, there is a problem that the reliability in respect of a function is spoiled that it is easy to become inadequate radiating heat. this invention was made in view of the above trouble, and aims at offer of the semiconductor device with which mounting with high high density and reliability was constituted by the wiring substrate (circuit board) possible.
[0007]
[Means for Solving the Problem] The 1st semiconductor chip to which the semiconductor device concerning this invention has the 1st bump electrode on a bonding pad, It has the 2nd bump electrode higher than the sum with the height of ** of the 1st semiconductor chip of the above, and the 1st bump electrode on a bonding pad. And the 2nd semiconductor chip which the active element field forming face was made to counter mutually on the field in which the 2nd bump electrode was formed, and carried out flip chip mounting of 1st at least one semiconductor chip, It has the 3rd bump electrode higher than the sum

with the height of ** of the 2nd semiconductor chip of the above, and the 2nd bump electrode on a bonding pad. And the 3rd semiconductor chip which an active element field forming face is made to counter mutually on the field in which the 3rd bump electrode was formed, and carries out flip chip mounting of 2nd at least one semiconductor chip is provided, and it is characterized by the bird clapper.

[0008] In the composition of the aforementioned semiconductor device, flip chip mounting of the 3rd semiconductor chip which accomplishes the composition which applied correspondingly above is carried out in the 4th semiconductor chip side, and the composition of flip chip mounting profit and still multilayer-arrangement can take the 4th semiconductor chip to the 5th semiconductor chip side similarly. And it is also possible to attach at least one sort, such as a chip resistor, a chip capacitor, a thin film resistor, and a thin film capacitor, to the semiconductor chip side which constitutes this semiconductor device, and such a thing is desirable from points, such as miniaturization of circuitry.

[0009]

[Function] According to the semiconductor device concerning this invention, compared with the case of flip chip mounting usually performed in the semiconductor chip in order to take the multi-stage composition which it was, and was carried out and carried out flip chip mounting in laminating, high density assembly can be easily attained in the composition of a mounting circuit apparatus. That is, since the wiring substrate area which mounting of a semiconductor device takes is sharply reduced compared with the superficial whole surface product of the semiconductor chip which forms the aforementioned semiconductor device, high-density-assembly-ization is realizable. And since it is not necessary to form a bonding pad in the rear face of a semiconductor chip, since good heat dissipation nature was held and demonstrated, when a mounting circuit apparatus is constituted, it not only also simplifies composition, but it presents a reliable function.

[0010]

[Example] The following, drawing 1 , and drawing 2 (a) - (j) The example of this invention is explained with reference to drawing 3 , drawing 4 , and drawing 5 .

[0011] Drawing 1 is the cross section of the example of important section composition of the semiconductor device concerning this invention. In this drawing 1 , 3 is the wiring substrate which mounted the semiconductor device 5 concerning this invention, and the aforementioned semiconductor device 5 is constituted as follows. The 1st semiconductor chip which has 1st bump electrode 6a on a bonding pad Namely, 5a, It has 2nd bump electrode 6b higher than ** of semiconductor chip 5a of the above 1st, and the sum of the 1st bump electrode 6a height on a bonding pad. And active element field 7a and 7b forming face are made to counter mutually in the field (on a field) in which 2nd bump electrode 6b was formed. The 2nd semiconductor chip 5b which carried out flip chip mounting of the semiconductor chip 5a of the above 1st, It has 3rd bump electrode 6c higher than ** of semiconductor chip 5b of the above 2nd, and the sum of the 2nd bump electrode 6b height on a bonding pad. And active element field 7b and 7c forming face were made to counter mutually in the field in which 3rd bump electrode 6c was formed, and the composition of having provided 3rd semiconductor chip 5c which carried out flip chip mounting of the semiconductor chip 5b of the above 2nd is accomplished.

[0012] And the semiconductor device 5 of the aforementioned composition can be easily manufactured by the following meanses. Drawing 2 (a) - (j) It is what showed typically the example of an embodiment which manufactures a semiconductor device 5, and first, bonding pad 8b prepares 2nd semiconductor chip 5b formed in the field to which some passivation films were removed, and exposes bonding pad 8b page to the aforementioned bonding pad 8b forming face of this 2nd semiconductor chip 5b, for example, prepares polyimide resin layer 9b. Formation of this polyimide resin layer 9b is for example, a polyimide precursor. It exposes, after carrying out the spin coat of UR-3140 (the Toray Industries make, tradename) to the whole surface, and it is a developer. After developing negatives by DV505 (the Toray Industries make, tradename) and carrying out opening of the bonding pad 8b page, it heats at the temperature of about 400 degrees C, and it is a polyimide precursor. UR-3140 school is made to polyimide-ize (drawing 2 (a

[0013] Subsequently, it is an etching resist on the aluminum/Ti stratification plane vacuum evaporationo and after forming about a aluminum/Ti layer on polyimide resin layer 9 the b-th page formed above. An OFPR-800 spin (Tokyo adaptation company) coat is carried out, and the etching-resist pattern which connects prebaking, exposure, and development to deed aforementioned bonding pad 8b one by one is formed. thus, the mixed liquor of the phosphoric acid after forming an etching-resist pattern / acetic acid / nitric acid -- aluminum -- EDTA/NH3 / H2 O2 Ti -- ** -- after carrying out selective etching one by one, the aforementioned etching-resist pattern is accomplished OFPR-800 a layer -- removing -- 2nd wiring putter 10b is formed ( drawing 2 (b)).

[0014] The 2nd circuit pattern of the above On the field in which 10b was formed, it is the 2nd bonding pad like the aforementioned case about polyimide resin layer 9c. It forms except for the portion equivalent to 11a (drawing 2 (c)). On the field in which the aforementioned polyimide resin layer 9c was formed, the Ti/Cu layer 13 is formed by vacuum evaporationo ( drawing 2 (d)). Subsequently, it is a thick-film resist on the 12th page of the Ti/Cu layer which carried out [ aforementioned ] formation. The spin coat of AZ 4903 (Hoechst Japan make) is carried out, and it is thickness. 500 micrometers The resist layer 13 of a grade is formed and exposure and development are performed one by one. From bonding pad 9b which has opening of 100 micrometer **, one side is 20 micrometers. Small 80 micrometers Opening 14 is formed (drawing 2 (e)). Copper-sulfate 250 g/l and a sulfuric acid (specific gravity 1.84) after carrying out [ aforementioned ] masking It is current density, flooding with the solution which consists of 50 g/l, setting it as the degree of bath temperature of 25 degrees C, and using high grade copper as an anode plate by using the aforementioned Ti/Cu layer 12 as cathode. 5 A/dm2 It is copper, impressing and stirring gently. 450 micrometers It plates. Then, the plating bath which consists of all tin 40 g/l, 1st tin 35 g/l, lead 44 g/l, isolation boric-acid 40 g/l, boric-acid 25 g/l, and glue 3.0 g/l is used. It is current density, using cathode and 40%

SUZU ** as an anode plate for the aforementioned Ti/Cu layer 12. 3.2 A/dm2 It is 50 micrometers about the alloy of tin / lead =40/60, impressing and stirring gently. Continuation plating (drawing 2 (f)) is carried out, and 2nd bump 6b is formed.
[0015] Thick-film resist which had accomplished the plating resist film after forming 2nd bump 6b with the above 4903 layer of AZ(s) 13 After carrying out dissolution removal with an acetone (drawing 2 (g)), with for example, the solution which consists of an ammonium persulfate / sulfuric acid / ethanol by using the aforementioned tin / lead (2nd bump) 6b as an etching mask The exposed aforementioned Ti layer is **********ed after etching the exposed aforementioned Cu layer with the solution which consists of EDTA, ammonia, and a hydrogen peroxide further, and dissolution removal of the resist OFPR layer 9c is carried out with an acetone after that ( drawing 2 (h)).
[0016] On the other hand, it consists of operations to which 1st semiconductor chip 5a also applied correspondingly above. That is, bonding pad 8a prepares 1st semiconductor chip 5a formed in the field to which some passivation films were removed. Here, as the 1st semiconductor chip 5a, the configuration and a size can contain and arrange in the bump electrode 6b field of semiconductor chip 5b of the above 2nd. Bonding pad 8a page is exposed to the aforementioned bonding pad 8a forming face of this 1st semiconductor chip 5a, polyimide resin layer 9a is prepared, and the vacuum evaporationo and formation of a Cu/Ti layer are done on this polyimide resin layer 9 b-th page. Then, it is a thick-film resist on the aforementioned Cu/Ti stratification plane. The spin coat of AZ 4903 (Hoechst Japan make) is carried out, and it is 50 micrometers of thickness. One side is 20 micrometers for example, from size [ of bonding pad 8a / of 80 micrometers ] ** about the field corresponding to [ form the resist layer of a grade, perform exposure and development one by one, and ] the aforementioned bonding pad 8a page. Opening is carried out to small 60 micrometer **. Thus, copper-sulfate 250 g/l and a sulfuric acid (specific gravity 1.84) after masking It is current density, flooding with the solution which consists of 50 g/l, setting it as the degree of bath temperature of 25 degrees C, and using high grade copper as an anode plate by using the aforementioned Ti/Cu layer as cathode. 5 A/dm2 It is 40 micrometers about copper, impressing and stirring gently. It plates. Then, cathode and 40% SUZU ** are used as an anode plate for the aforementioned Ti/Cu layer using the plating bath which consists of all tin 40 g/l, 1st tin 35 g/l, lead 44 g/l, isolation boric-acid 40 g/l, boric-acid 25 g/l, and glue 3.0 g/l. Current density 3.2 A/dm2 It is 10 micrometers about the alloy of tin / lead =40/60, impressing and stirring gently. Continuation plating is carried out and necessary bump electrode 6a is formed.
[0017] Thick-film resist which had accomplished the plating resist film after forming bump electrode 6a with the above After carrying out dissolution removal of the 4903 layer of the AZ(s) with an acetone, the aforementioned tin / lead (1st bump) 6a are used as an etching mask. With the solution which consists of EDTA, ammonia, and a hydrogen peroxide further after etching the exposed aforementioned Cu layer with the solution which consists of an ammonium persulfate / sulfuric acid / ethanol The exposed aforementioned Ti layer is **********ed, dissolution removal of the resist OFPR layer is carried out with an acetone after that, and 1st semiconductor chip 5a is obtained.
[0018] Furthermore, 3rd semiconductor chip 5c is manufactured according to the manufacturing process of 1st semiconductor chip of the above 5a, and 2nd semiconductor chip 5b. The 3rd bonding pad 11b by which the configuration and a size can contain and arrange semiconductor chip 5b of the above 2nd as the 3rd semiconductor chip 5c in the composition of this 3rd semiconductor chip 5c in the field of protruding bump electrode 6c, and bump electrode 6of semiconductor chip 5b of the above 2nd b is connected to the active element field 7c page It is formed. Furthermore, it is set up more than the height which can also contain and arrange the height of the aforementioned bump electrode 6c which carries out a protrusion in the form which carries out the interior (built-in) of the semiconductor chip 5b of the above 2nd into the field of bump electrode 6c, i.e., the thickness of 2nd semiconductor chip 5b, and the sum with the height of the bump electrode 6b.
[0019] Next, bump electrode 6b and 2nd bonding pad 11a necessary to an aforementioned active element field 7b top To up to 2nd semiconductor chip 5b prepared, this 2nd semiconductor chip 5b is received. Maintaining 1st semiconductor chip 5a at the physical relationship of a face down About bump electrode 6of 1st semiconductor chip 5a a, it is 2nd bonding pad 11a of 2nd semiconductor chip 5b. Alignment is carried out using a one-way mirror, and they are these bumps electrode 6a and 2nd bonding pad 11a. It is made to opposite-**. In addition, it sets at this process and they are aforementioned bump electrode 6a and 2nd bonding pad 11a. The eutectic-solder layer is made to be beforehand placed between the fields which opposite-**, and 1st semiconductor chip 5a is held to the collet of heating mechanism attachment, and the aforementioned operation is performed. And bump electrode 6of semiconductor chip 5a of the above 1st a and 2nd bonding pad 11a of 2nd semiconductor chip 5b It is in the state made to opposite-**, for example, both are electrically connected the inside of nitrogen atmosphere, and by heating at about 280 degrees C ( drawing 2 (i)).
[0020] After carrying out flip chip mounting of the 1st semiconductor chip 5a with the above at 2nd semiconductor chip 5b, the semiconductor device concerning this invention is constituted by [ which carry out flip chip mounting of the 2nd semiconductor chip 5b this 1st semiconductor chip 5a was made to mount further at 3rd semiconductor chip 5c according to the aforementioned mounting means ( drawing 2 (j)) ] carrying out.
[0021] It sets in the aforementioned composition and is 1st semiconductor chip 5a. 3mm**, the five b4mm [ of 2nd semiconductor chip ] **, and 1st semiconductor chip 5c The semiconductor device which sets it as 5mm**, respectively and turns to it the case of the mounting circuit apparatus constituted from a conventional wire bonding method when it mounted in the wiring substrate side and the mounting circuit apparatus was constituted -- comparing -- packaging density 5 times -- moreover -- the case of the mounting circuit apparatus constituted from a TAB method -- comparing -- packaging density It was improving by 4 times, respectively. Furthermore, when the thermal resistance of a semiconductor device is evaluated, 40 degrees C/W in composition of being 20-degree-C/W with the chip of 5mm**, and having carried out the laminating by the wire bonding method by natural air cooling, (refer to drawing 7 ) is received. The thermolysis property of double precision

was shown. Moreover, the increase in the Yukinari **** result and connection resistance was not accepted in the composition shown in drawing 1 about the mounting circuit apparatus which carried out flip chip mounting in a 25 degrees C (5 min) - 150 degree C [ -55 degree C (30 min) to ] (30 min) - 25 degrees C (5 min) heat cycle test (1000 cycles), but high reliability was shown also in respect of the function.

[0022] It is what showed other examples of important section composition of the semiconductor device concerning this invention in cross section, it sets in this composition, and drawing 3 is a CCD chip to a glass-substrate 3' side instead of a wiring substrate. It is a driver IC about 15a. Bump electrode of 15b In the form which carries out interior into the field of 16b, it is a CCD chip. 15a and driver IC The composition which carried out FURIBBU chip mounting of the 15b, respectively is taken. Since the signal which received light through glass-substrate 3' was controllable by driver-IC 15b, compared with the case of the composition using the conventional flexible substrate, the miniaturization of electronic equipment of the case of this semiconductor device was also attained.

[0023] Furthermore, drawing 4 is what showed another example of important section composition of the semiconductor device concerning this invention in tropia, and, in them, 1st semiconductor chip 5a is carrying out flip chip mounting on the 3rd semiconductor chip 5 c-th page in this example of composition. [ two or more ] 8c is the 3rd bonding pad and 11b by which 3rd bump electrode 6c is prepared in the upper surface in drawing 4 . It is the 2nd bonding pad which bump electrode 6of 2nd semiconductor chip 5b b etc. connects. The densification of the semiconductor chip in a semiconductor device is possible, and in the 3rd semiconductor chip 5c page, in this composition, a chip resistor, a chip capacitor, a thin film resistor, a thin film capacitor, etc. are combined, and it is easy to mount it.

[0024] Drawing 5 is what showed in tropia the example of important section composition from which the semiconductor device concerning this invention differs, and is carrying out flip chip mounting in this example of composition further again, for example in the form where 1st semiconductor chip 5a was made to cross on the 3rd semiconductor chip 5 c-th page. That is, in the semiconductor device concerning this invention, the composition which carried out flip chip mounting (** which does not arrange the sense) can be taken to arbitrary sense according to configurations, such as semiconductor chips 5a, 5b, and 5c, (without restraining the configuration of a semiconductor chip).

[0025] In addition, this invention is not limited to the aforementioned example, is changed in the range which does not deviate from the summary, and can be carried out. For example, the conductive layer of it not being limited to Cu/Ti and the number of semiconductor chips which carries out flip chip mounting still in multi-stage not being limited to the aforementioned instantiation, either which may perform formation of a bump electrode with other Au(s) of Cu, Pd, Pt, nickel, etc., and accomplishes cathode by electroplating at the time of formation of a bump electrode is also natural.

[0026]

[Effect of the Invention] Since a wiring substrate side can be used in three dimensions compared with the case where a semiconductor mounting circuit apparatus is constituted, by semiconductor device ****** and the conventional flip chip mounting concerning this invention, it becomes realizable [ a high-density-assembly circuit apparatus ]. And on the other hand, while being able to attain reliable electric connection, without requiring complicated work etc. in this densification achievement compared with the method learned conventionally, since good thermolysis nature is presented, it is reliable and composition of a high-density-assembly circuit apparatus can be aimed at easily.

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[Translation done.]

* NOTICES *



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2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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CLAIMS

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[Claim(s)]
[Claim 1] The semiconductor device characterized by providing the following. The 1st semiconductor chip which has the 1st bump electrode on a bonding pad. The 2nd semiconductor chip which the active element field forming face was made to counter mutually on the field where it has the 2nd bump electrode higher than the sum with the height of ** of the 1st semiconductor chip of the above, and the 1st bump electrode, and the 2nd bump electrode was formed on the bonding pad, and carried out flip chip mounting of 1st at least one semiconductor chip. The 3rd semiconductor chip which the active element field forming face was made to counter mutually on the field where it has the 3rd bump electrode higher than the sum with the height of ** of the 2nd semiconductor chip of the above, and the 2nd bump electrode, and the 3rd bump electrode was formed on the bonding pad, and carried out flip mounting of 2nd at least one semiconductor chip.

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[Translation done.]

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The cross section showing the example of important section composition of the semiconductor device concerning this invention.
[Drawing 2] It is what shows typically the example of an embodiment which manufactures the semiconductor device concerning this invention. (a) The cross section and (b) which show the state where the insulating layer was formed in the semiconductor chip side The cross section showing the state where the circuit pattern was formed on the insulating layer, (c) The cross section and (d) which show the state where the 2nd bonding pad was formed The cross section showing the state where the conductive layer for plating was formed, The cross section showing the state where (e) carried out patterning of the plating resist film, (f) The cross section and (g) which show the state where plating formation of the bump electrode was carried out The cross section showing the state where the plating resist film was removed, (h) The cross section showing the state where the 2nd bonding pad was formed, and (i) are the cross section showing the state where FURIBBU chip mounting of the 1st semiconductor chip was carried out in the 2nd semiconductor chip side, and (j). Cross section of a semiconductor device.
[Drawing 3] The cross section showing other examples of important section composition of the semiconductor device concerning this invention.
[Drawing 4] The cross section showing another example of important section composition of the semiconductor device concerning this invention.
[Drawing 5] The cross section showing another example of important section composition of the semiconductor device concerning this invention.
[Drawing 6] The cross section showing the mode which mounted the conventional semiconductor device in the wiring substrate side.
[Drawing 7] The cross section showing other modes which mounted the conventional semiconductor device in the wiring substrate side.
[Description of Notations]
1a, 1b, 1c -- Semiconductor chip 2a, 2b, 2c -- Bonding pad 3 -- Wiring substrate 3' -- Glass substrate 4 -- Bonding wire 5 -- Semiconductor device 5a -- The 1st semiconductor chip 5b -- The 2nd semiconductor chip 5c -- The 3rd semiconductor chip 6a -- 1st bump electrode 6b -- 2nd bump electrode 6c -- 3rd bump electrode
7a, 7b, 7c -- Active element field 8a, 8b, 8c -- Bonding pad 9a, 9b, 9c -- Polyimide resin layer 10a -- Circuit pattern 11a and 11b -- The 2nd bonding pad 12 -- Ti/Cu layer 13 -- Resist layer 14 -- Opening 15a -- CCD Chip
15b -- Driver IC 16a -- CCD Bump electrode of a chip 16b -- Bump electrode of a driver IC

* NOTICES *



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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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DRAWINGS

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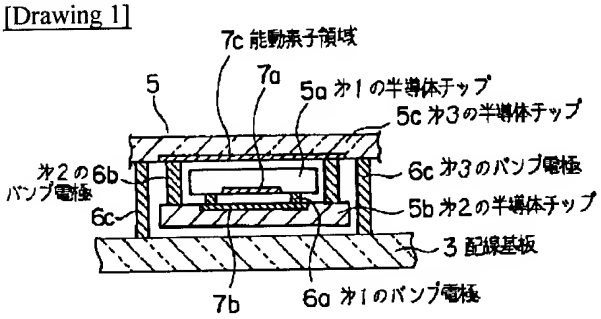
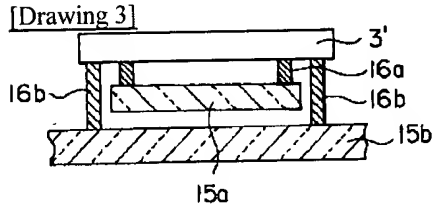
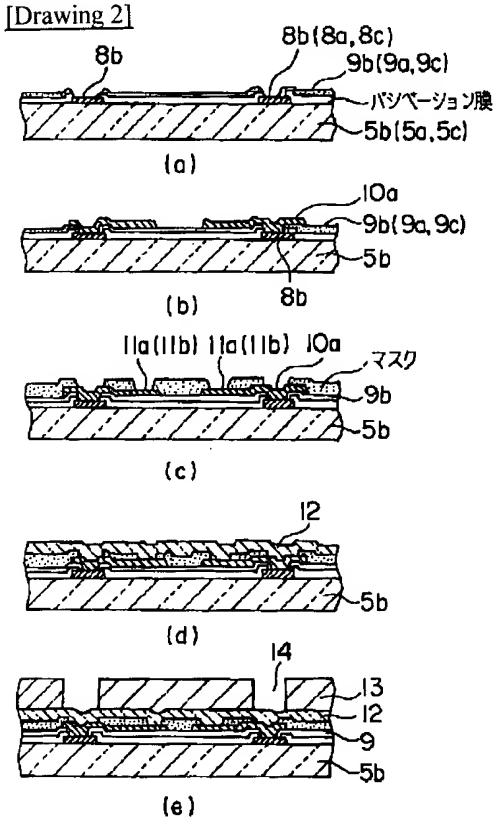
[Drawing 1]

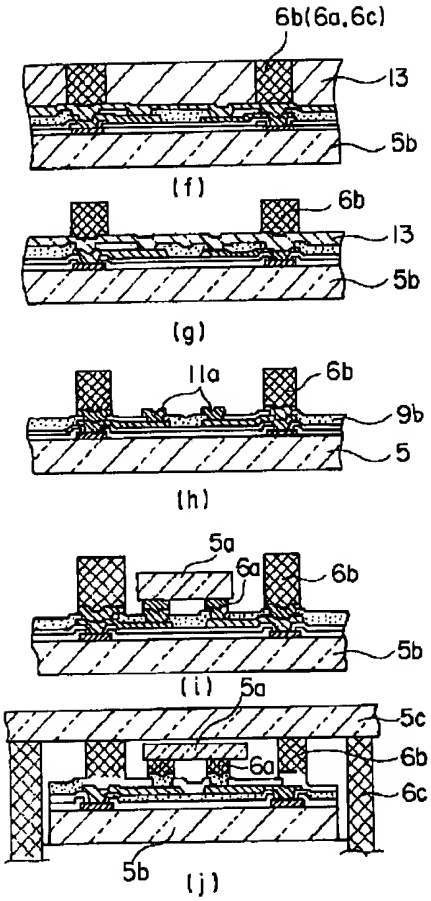



[Drawing 3]

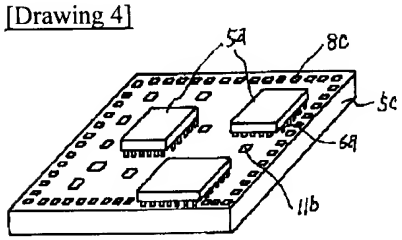



[Drawing 2]






[Drawing 4]

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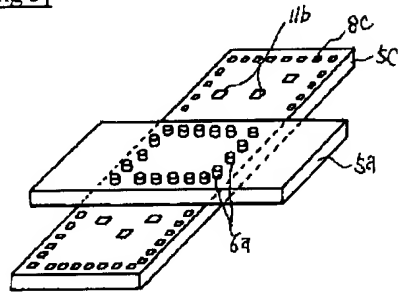
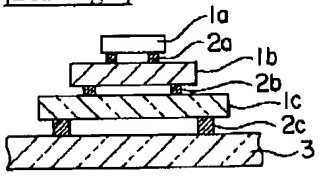
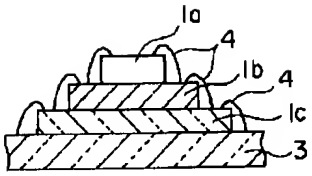



[Drawing 6]




[Drawing 7]




[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報**（Ａ）　(11)特許出願公開番号

特開平6－132474

(43)公開日　平成６年(1994)５月13日

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| 25/07 | | | | |
| 25/18 | | | | |
| | | | Ｈ０１Ｌ 25/ 08 | Ｂ |

審査請求　未請求　請求項の数１(全 ７ 頁)

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(22)出願日　平成４年(1992)３月18日

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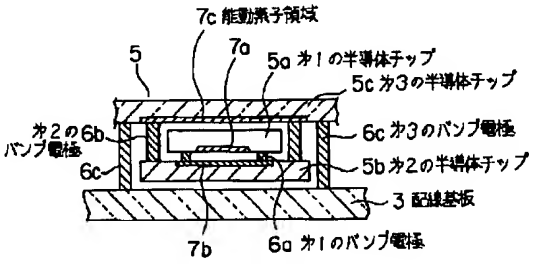
(54)【発明の名称】　半導体装置

(57)【要約】

【目的】　配線基板（回路基板）に、高密度かつ信頼性の高い実装が可能に構成された半導体装置の提供を目的とする。

【構成】　ボンデングパッド8a上に第１のバンプ電極6aを有する第１の半導体チップ5aと、ボンデングパッド8b上に前記第１の半導体チップ5aの厚および第１のバンプ電極6aの高さの和よりも高い第２のバンプ電極6bを有し、かつ第２のバンプ電極5bが形成された面上において互いに能動素子領域7a，7b形成面を対向させて少なくとも１個の第１の半導体チップ5aをフリップチップ実装した第２の半導体チップ5bと、ボンデングパッド8c上に前記第２の半導体チップ5bの厚および第２のバンプ電極6bの高さの和よりも高い第３のバンプ電極6cを有し、かつ第３のバンプ電極6cが形成された面上において互いに能動素子領域7b，7c形成面を対向させて少なくとも１個の第２の半導体チップ5bをフリップ実装する第３の半導体チップ5cとを具備してなることを特徴し、３層以上の多層型に構成されている。



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【特許請求の範囲】

【請求項1】　ボンデングパッド上に第1のバンプ電極を有する第1の半導体チップと、ボンデングパッド上に前記第1の半導体チップの厚および第1のバンプ電極の高さとの和よりも高い第2のバンプ電極を有し、かつ第2のバンプ電極が形成された面上において互いに能動素子領域形成面を対向させて少なくとも1個の第1の半導体チップをフリップチップ実装した第2の半導体チップと、ボンデングパッド上に前記第2の半導体チップの厚および第2のバンプ電極の高さとの和よりも高い第3のバンプ電極を有し、かつ第3のバンプ電極が形成された面上において互いに能動素子領域形成面を対向させて少なくとも1個の第2の半導体チップをフリップ実装した第3の半導体チップとを具備してなることを特徴とする半導体装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は半導体装置に係り、特に複数の半導体チップを高密度に配線基板面への実装を可能に構成した半導体装置に関する。

【0002】

【従来の技術】半導体装置（半導体チップもしくは半導体素子）は近年高集積化の方向にあり、またこの種の半導体装置を高密度に配線基板へ実装する要求も高まっている。そして、半導体装置を配線基板面へ、高密度に実装する手段として、様々な方法も提案されているが、最近は主にフリップチップ実装方法が行われている。フリップチップ実装は、ワイヤーボンデング実装やTAB実装に比較して、半導体チップを高密度に実装できるからである。すなわち、ワイヤーボンデング実装やTAB実装によって、半導体チップを実装した場合は、半導体チップから引き出されるリードの占める面積が、半導体チップの2～3倍の面積を必要とする。一方、フリップチップ実装の場合、半導体チップの実装面積は半導体チップの面積で足り、半導体チップを互いに隣接した上体で実装し得る。したがって、フリップチップ実装に比較すると、ワイヤーボンデング実装やTAB実装は半導体チップの実装面積が1/2～1/3程度となり、高密度化の限界をなしている。

【0003】ところで、前記フリップチップ実装は、いわゆる平面実装であるため、実装密度も配線基板面から制約を受け、実装の高密度化にも限界がある。このような問題に対して、たとえばIMC 90 Proceedingに記載されているごとく、TAB実装のテープキャリアを積層して、半導体チップを3次元に実装する手段、あるいはEP&P 1990 p76に記載されているように、半導体チップを縦方向に並べて3次元的に実装する手段が提案されている。

【0004】

【発明が解決しようとする課題】しかしながら、前記3

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次元（的）実装の場合は、たとえばメモリチップのように実装する半導体チップのサイズが同一でなかったり、あるいは形状が不均一であったりすると、目的に沿った実装の高密度化を達成し得ないという問題がある。

【0005】一方、サイズの異なる半導体チップを、図6に断面的に示すごとく多段的に実装する構成も試みられている。すなわち、サイズの異なる各半導体チップ1a，1b，1cについて、それぞれ能動素子領域面のボンデングパッドから裏面側に配線を引き伸し、裏面に第2のボンデイングパッド2a，2b，2cを設け、これら第2のボンデイングパッド2a，2b，2cを介して、配線基板3面に各半導体チップ1a，1b，1cを多段的に実装した構成を採っている。しかし、この構成においては、半導体チップ1a，1b，1cの裏面に、第2のボンデイングパッド2a，2b，2cを設けることが困難であり、また半導体チップ1a，1b，1cに孔を穿設し、この孔を利用して第2のボンデイングパッド2a，2b，2cを設けるとしても、前記孔の穿設工程を要する。いずれにしても、この図6に図示した構成の場合は、コストアップとなるなど問題がある。

【0006】さらに、サイズの異なる半導体チップを、図7に断面的に示すごとく多段的に積層・配置する構成も試みられている。すなわち、サイズの異なる各半導体チップ1a，1b，1cを、能動素子領域面を上面として所要の配線基板3面に、順次積層的にマウントするとともに、相互の間をワイヤボンデング4により電気的に接続して実装した構成を採っている。しかし、この構成においては、半導体チップ1a，1b，1cの発熱面をなす能動素子領域面上に他の半導体チップがマウントされるため、放熱が不十分となり易く機能面での信頼性が損なわれるという問題がある。　本発明は以上の問題点に鑑みてなされたもので、配線基板（回路基板）に、高密度かつ信頼性の高い実装が可能に構成された半導体装置の提供を目的とする。

【0007】

【課題を解決するための手段】本発明に係る半導体装置は、ボンデングパッド上に第1のバンプ電極を有する第1の半導体チップと、ボンデングパッド上に前記第1の半導体チップの厚および第1のバンプ電極の高さとの和よりも高い第2のバンプ電極を有し、かつ第2のバンプ電極が形成された面上において互いに能動素子領域形成面を対向させて少なくとも1個の第1の半導体チップをフリップチップ実装した第2の半導体チップと、ボンデングパッド上に前記第2の半導体チップの厚および第2のバンプ電極の高さとの和よりも高い第3のバンプ電極を有し、かつ第3のバンプ電極が形成された面上において互いに能動素子領域形成面を対向させて少なくとも1個の第2の半導体チップをフリップチップ実装する第3の半導体チップとを具備してなることを特徴とする。

【0008】前記半導体装置の構成においては、上記に準じた構成を成す第3の半導体チップを第4の半導体チ

ップ面にフリップチップ実装し、同様に第４の半導体チップを第５の半導体チップ面にフリップチップ実装ごとく、さらに多層的な配置の構成も採り得る。そして、この半導体装置を構成する半導体チップ面に、たとえばチップ抵抗，チップコンデンサ，薄膜抵抗，薄膜コンデンサなどの、少なくとも１種を付設しておくことも可能で、こうしたことは回路構成のコンパクト化などの点から好ましい。

【０００９】

【作用】本発明に係る半導体装置によれば、半導体チップを多段的ないし積層的にフリップチップ実装した構成を採るため、通常行われているフリップチップ実装の場合に比べて、実装回路装置の構成において高密度実装を容易に達成し得る。すなわち、半導体装置の実装に要する配線基板面積は、前記半導体装置を形成する半導体チップの平面的な全面積に比べて大幅に低減するため、高密度実装化を実現できる。しかも、半導体チップの裏面にボンデングパッドを設ける必要もないので、構成も簡略化するばかりでなく、良好な放熱性を保持・発揮するので実装回路装置を構成したときも、信頼性の高い機能を呈する。

【００１０】

【実施例】以下、図１、図２(a) ～(j) 、図３、図４および図５を参照して本発明の実施例を説明する。

【００１１】図１は本発明に係る半導体装置の要部構成例の断面図である。この図１において、３は本発明に係る半導体装置５を実装した配線基板で、前記半導体装置５は、次のように構成されている。すなわち、ボンデングパッド上に第１のバンプ電極6aを有する第１の半導体チップは5a、ボンデングパッド上に前記第１の半導体チップ5aの厚および第１のバンプ電極6a高さの和よりも高い第２のバンプ電極6bを有し、かつ第２のバンプ電極6bが形成された面（面上）において互いに能動素子領域7a，7b形成面を対向させて、前記第１の半導体チップ5aをフリップチップ実装した第２の半導体チップ5b、ボンデングパッド上に前記第２の半導体チップ5bの厚および第２のバンプ電極6b高さの和よりも高い第３のバンプ電極6cを有し、かつ第３のバンプ電極6cが形成された領域内において互いに能動素子領域7b，7c形成面を対向させて、前記第２の半導体チップ5bをフリップチップ実装した第３の半導体チップ5cとを具備した構成を成している。

【００１２】そして、前記構成の半導体装置５は、次のような手段によって容易に製造し得る。図２(a) ～(j) は、半導体装置５を製造する実施態様例を模式的に示したもので、先ず、ボンデングパッド8bが、パッシベーション膜の一部が除かれた領域に形成された第２の半導体チップ5bを用意し、この第２の半導体チップ5bの、前記ボンデングパッド8b形成面に、ボンデングパッド8b面を露出させて、たとえばポリイミド樹脂層9bを設ける。こ



のポリイミド樹脂層9bの形成は、たとえばポリイミド前駆体 UR-3140（東レ製，商品名）を全面にスピンコートした後、露光し、現像液 DV505（東レ製，商品名）により現像して、ボンデングパッド8b面を開口してから、４００℃程度の温度で加熱してポリイミド前駆体 UR-3140校をポリイミド化させる（図２(a)）。

【００１３】次いで、前記で形成したポリイミド樹脂層9b面上に、Al／Ti層を蒸着・形成した後、そのAl／Ti層面上にエッチングレジスト OFPR-800（ 東京応化社）スピンコートし、プリベーク，露光，現像を順次行い前記ボンデングパッド8bに接続するエッチングレジストパターンを形成する。このように、エッチングレジストパターンを形成した後、リン酸／酢酸／硝酸の混合液でAlを、EDTA／$NH_3$ ／ $H_2$ $O_2$ でTiをと順次選択エッチングしてから、前記エッチングレジストパターンを成す OFPR-800 層を除去して、第２の配線パター 10bを形成する（図２(b)）。

【００１４】前記第２の配線パターン 10bを形成した面上に、ポリイミド樹脂層9cを前記の場合と同様にして、第２のボンデングパッド 11aに相当する部分を除いて形成する（図２(c)）。前記ポリイミド樹脂層9cを形成した面上に、たとえばTi／Cu層13を蒸着によって形成する（図２(d)）。次いで、前記形成したTi／Cu層12面上に、厚膜レジスト AZ 4903（ヘキストジャパン社製）をスピンコートして、膜厚 500$\mu$m 程度のレジスト層13を形成し、露光，現像を順次行って 100$\mu$m □の開口を有するボンデングパッド9bよりも、一辺が20$\mu$m 小さい80$\mu$m の開口部14を形成する（図２(e)）。前記マスキングした後、硫酸銅250g/l，硫酸（比重1.84） 50g/lから成る溶液に浸漬して、浴温度25℃に設定し、前記Ti／Cu層12を陰極，高純度銅を陽極として、電流密度 5A/$dm^2$ を印加して緩やかに撹拌しながら銅を 450$\mu$m メッキする。その後、全スズ40 g/l，第１スズ35 g/l，鉛44 g/l，遊離ホウ酸40 g/l，ホウ酸25 g/l，ニカワ3.0g/lから成るメッキ浴を用い、前記Ti／Cu層12を陰極，40%スズをを陽極として、電流密度 3.2A/$dm^2$ を印加して緩やかに撹拌しながらスズ／鉛＝40／60の合金を50$\mu$m 連続メッキ（図２(f)）して、第２のバンプ6bを形成する。

【００１５】前記により第２のバンプ6bを形成した後、メッキレジスト膜を成していた厚膜レジスト AZ 4903層13を、たとえばアセトンで溶解除去してから（図２(g)）、前記スズ／鉛（第２のバンプ）6bをエッチングマスクとして、過硫酸アンモニウム／硫酸／エタノールから成る溶液で、露出した前記Cu層をエッチング後、さらにEDTA，アンモニア，過酸化水素から成る溶液で、露出した前記Ti層をエッチングして、その後レジストOFPR層9cをアセトンで溶解除去する（図２(h)）。

【００１６】一方、第１の半導体チップ5aも前記に準じた操作で構成される。すなわち、ボンデングパッド8aが、パッシベーション膜の一部が除かれた領域に形成さ

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れた第１の半導体チップ5aを用意する。ここで、第１の半導体チップ5aとしては、その形状，大きさが前記第２の半導体チップ5bのバンプ電極6b領域内に収納・配置し得るものである。この第１の半導体チップ5aの、前記ボンデングパッド8a形成面に、ボンデングパッド8a面を露出させてポリイミド樹脂層9aを設け、このポリイミド樹脂層9b面上に、Cu／Ti層を蒸着・形成する。その後、前記Cu／Ti層面上に厚膜レジスト AZ 4903（ヘキストジャパン社製）をスピンコートして、膜厚50μm 程度のレジスト層を形成し、露光，現像を順次行い、前記ボンデングパッド8a面に対応した領域を、たとえばボンデングパッド8aの大きさ80μm □よりも、一辺が20μm 小さい60μm □に開口させる。このようにマスキングした後、硫酸銅250g/l，硫酸（比重1.84） 50g/lから成る溶液に浸漬して、浴温度25℃に設定し、前記Ti／Cu層を陰極，高純度銅を陽極として、電流密度 5A/dm² を印加して緩やかに撹拌しながら銅を40μm メッキする。その後、全スズ40 g/l，第１スズ35g/l，鉛44 g/l，遊離ホウ酸40 g/l，ホウ酸25 g/l，ニカワ3.0g/lから成るメッキ浴を用い、前記Ti／Cu層を陰極，40％スズをを陽極として、電流密度 3.2A/dm² を印加して緩やかに撹拌しながらスズ／鉛＝40／60の合金を10μm 連続メッキして、所要のバンプ電極6aを形成する。

【００１７】前記によりバンプ電極6aを形成した後、メッキレジスト膜を成していた厚膜レジスト AZ 4903層を、たとえばアセトンで溶解除去してから、前記スズ／鉛（第１のバンプ）6aをエッチングマスクとして、過硫酸アンモニウム／硫酸／エタノールから成る溶液で、露出した前記Cu層をエッチング後、さらにEDTA，アンモニア，過酸化水素から成る溶液で、露出した前記Ti層をエッチングして、その後レジストOFPR層をアセトンで溶解除去し、第１の半導体チップ5aを得る。

【００１８】さらに、前記第１の半導体チップ5aおよび第２の半導体チップ5bの製造工程に準じて、第３の半導体チップ5cを製造する。この第３の半導体チップ5cの構成においては、第３の半導体チップ5cとしてその形状，大きさが、前記第２の半導体チップ5bを、突設するバンプ電極6cの領域内に収納・配置し得るものであり、またその能動素子領域7c面に、前記第２の半導体チップ5bのバンプ電極6bが接続される第３のボンデングパッド11b が形成される。さらに、前記突設するバンプ電極6cの高さも、前記第２の半導体チップ5bをバンプ電極6cの領域内に内装（内蔵）する形で収納・配置し得るような高さ、すなわち第２の半導体チップ5bの厚さおよびそのバンプ電極6bの高さとの和以上に設定される。

【００１９】次に、前記能動素子領域7b上に所要のバンプ電極6bおよび第２ボンデングパッド11a が設けられている第２の半導体チップ5b上へ、この第２の半導体チップ5bに対して、第１の半導体チップ5aをフェースダウンの位置関係に保ちながら、第１の半導体チップ5aのバンプ電極6aを、第２の半導体チップ5bの第２ボンデングパッド11a にハーフミラーを用いて位置合わせし、これらバンプ電極6aおよび第２ボンデングパッド11a に対接させる。なお、この工程においては、前記バンプ電極6aおよび第２ボンデングパッド11a が対接する面に、予め共晶半田層を介在させてあり、また第１の半導体チップ5aを加熱機構付けのコレットに保持して前記操作を行っている。そして、前記第１の半導体チップ5aのバンプ電極6aと第２の半導体チップ5bの第２ボンデングパッド11aとを対接させた状態で、たとえば窒素雰囲気中、 280℃程度に加熱することによって両者を電気的に接続する（図２(i)）。

【００２０】前記により第２の半導体チップ5bに、第１の半導体チップ5aをフリップチップ実装した後、この第１の半導体チップ5aを実装させた第２の半導体チップ5bを、前記実装手段に準じて、さらに第３の半導体チップ5cにフリップチップ実装する（図２(j)）することによって、本発明に係る半導体装置が構成される。

【００２１】前記構成において、第１の半導体チップ5aを 3mm□，第２の半導体チップ5bを4mm□，第１の半導体チップ5cを 5mm□ にそれぞれ設定して成る半導体装置を、配線基板面に実装して実装回路装置を構成したところ、従来のワイヤボンデング方式で構成した実装回路装置の場合に比べて実装密度が 5倍、また TAB方式で構成した実装回路装置の場合に比べて実装密度が 4倍にそれぞれ向上していた。さらに、半導体装置の熱抵抗を評価したところ、 5mm□ のチップで自然冷却により20℃/Wであり、ワイヤボンデング方式で積層した構成の場合（図７参照）の40℃/Wに対して 2倍の放熱特性を示した。また、図１に示す構成にフリップチップ実装した実装回路装置について、 -55℃(30 min)～25℃( 5 min)～ 150℃(30 min)～25℃( 5 min)の温度サイクル試験（1000サイクル）を行成った結果、接続抵抗の増加は認められず、機能面でも高い信頼性を示した。

【００２２】図３は本発明に係る半導体装置の他の要部構成例を断面的に示したもので、この構成においては、配線基板の代わりにガラス基板３′面に、 CCDチップ 15aをドライバーIC 15bのバンプ電極 16bの領域内に内装する形で、 CCDチップ 15aおよびドライバーIC 15bをそれぞれフリップチップ実装した構成を採っている。この半導体装置の場合は、ガラス基板３′を通して受光した信号をドライバーIC15bで制御できるため、従来のたとえばフレキシブル基板を用いた構成の場合に比べて、電子機器のコンパクト化も可能となった。

【００２３】さらに、図４は本発明に係る半導体装置の別の要部構成例を斜視的に示したもので、この構成例においては、第３の半導体チップ5c面上に第１の半導体チップ5aが複数個フリップチップ実装している。図４において、8cはその上面に第３のバンプ電極6cが設けられる第３のボンデングパッド、11b は第２の半導体チップ5b

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のバンプ電極6bなどが接続する第２のボンデングパッドである。この構成の場合は、半導体装置における半導体チップの高密度化が可能で、また第３の半導体チップ5c面に、たとえばチップ抵抗，チップコンデンサ，薄膜抵抗，薄膜コンデンサなども併せて実装し易い。

【００２４】さらにまた、図５は本発明に係る半導体装置の異なる要部構成例を斜視的に示したもので、この構成例においては、たとえば第３の半導体チップ5c面上に、第１の半導体チップ5aを交差させた形でフリップチップ実装している。つまり、本発明に係る半導体装置においては、半導体チップ5a，5b，5cなどの形状に応じて（半導体チップの形状が制約されることなく）、任意な向きに（向きを揃えずに）フリップチップ実装した構成を採り得る。

【００２５】なお、本発明は前記実施例に限定されるものでなく、その要旨を逸脱しない範囲で変更して実施し得る。たとえば、バンプ電極の形成はCuの他Au，Pd，Pt，Niなどで行ってもよく、またバンプ電極の形成時の電気メッキで陰極を成す導電性層もCu／Tiに限定されないし、さらに多段的にフリップチップ実装する半導体チップ数も、前記例示に限定されないことは勿論である。

【００２６】

【発明の効果】本発明に係る半導体装置よれば、従来のフリップチップ実装によって半導体実装回路装置を構成する場合に比べて、配線基板面を立体的に利用し得るため、高密度実装回路装置の実現が可能となる。しかも、この高密度化達成に当たり、従来知られている方式に比べて繁雑な作業なども要せずに、信頼性の高い電気的な接続を達成し得るとともに、一方では良好な放熱性を呈するので、信頼性の高い、かつ高密度実装回路装置の構成を容易に図り得る。

【図面の簡単な説明】

【図１】本発明に係る半導体装置の要部構成例を示す断面図。

【図２】本発明に係る半導体装置を製造する実施態様例を模式的に示すもので、(a) は半導体チップ面に絶縁層



を形成した状態を示す断面図、(b) は絶縁層上に配線パターンを形成した状態を示す断面図、(c) は第２のボンデングパッドを形成した状態を示す断面図、(d) はメッキ用の導電層を形成した状態を示す断面図、(e)はメッキレジスト膜をパターンニングした状態を示す断面図、(f) はバンプ電極をメッキ形成した状態を示す断面図、(g) はメッキレジスト膜を除去した状態を示す断面図、(h) は第２のボンデングパッドを形成した状態を示す断面図、(i)は第２の半導体チップ面に第１の半導体チップをフリップチップ実装した状態を示す断面図、(j) は半導体装置の断面図。

【図３】本発明に係る半導体装置の他の要部構成例を示す断面図。

【図４】本発明に係る半導体装置の別の要部構成例を示す断面図。

【図５】本発明に係る半導体装置の別の要部構成例を示す断面図。

【図６】従来の半導体装置を配線基板面に実装した態様を示す断面図。

【図７】従来の半導体装置を配線基板面に実装した他の態様を示す断面図。

【符号の説明】

1a，1b，1c…半導体チップ　2a，2b，2c…ボンデングパッド　3…配線基板　3′…ガラス基板　4…ボンデングワイヤ　5…半導体装置　5a…第１の半導体チップ　5b…第２の半導体チップ　5c…第３の半導体チップ

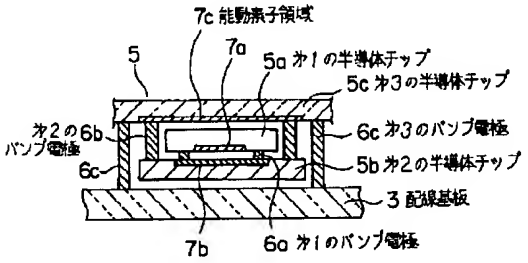
6a…第１のバンプ電極　6b…第２のバンプ電極　6c…第３のバンプ電極

7a，7b，7c…能動素子領域　8a，8b，8c…ボンデングパッド　9a，9b，9c…ポリイミド樹脂層　10a …配線パターン　11a,11b …第２のボンデングパッド

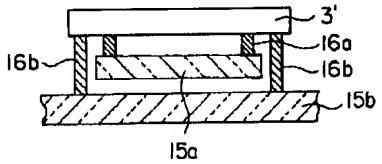
12…Ti／Cu層　13…レジスト層　14…開口部　15a …CCD チップ

15b …ドライバーIC　16a …CCD チップのバンプ電極　16b …ドライバーICのバンプ電極

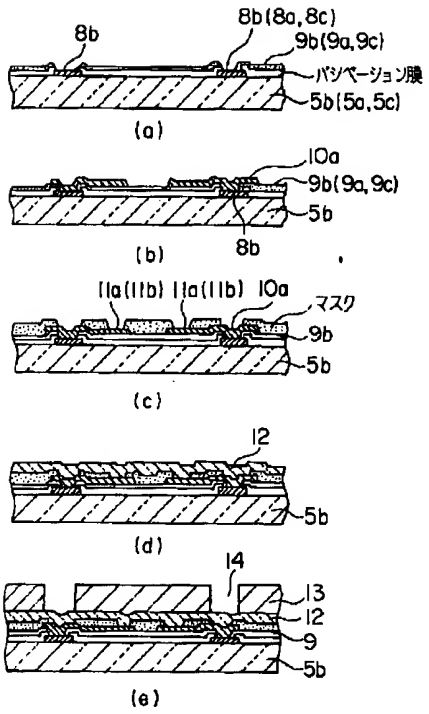
【図１】




【図３】



【図2】

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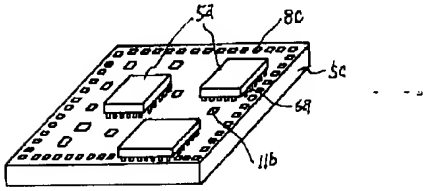
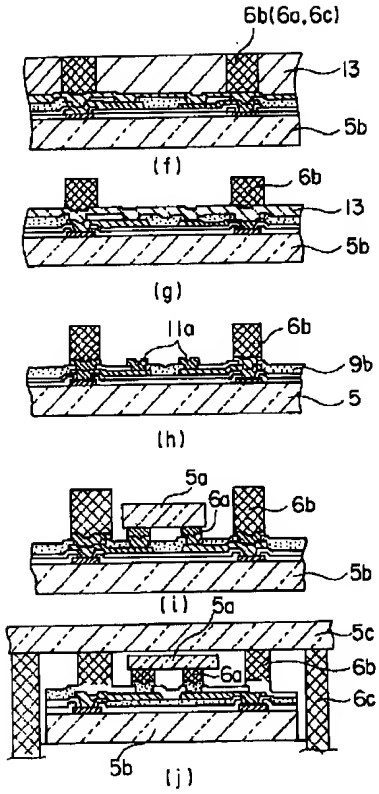
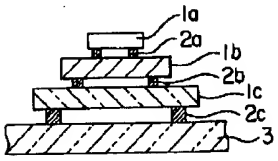
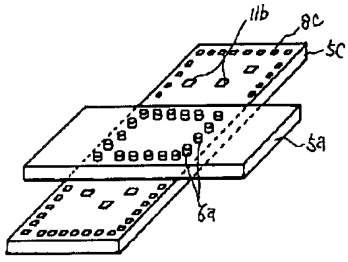


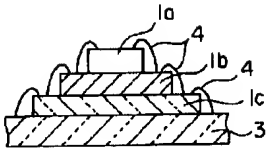

【図6】




【図5】




【図7】

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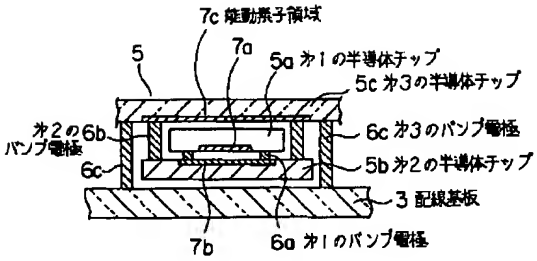
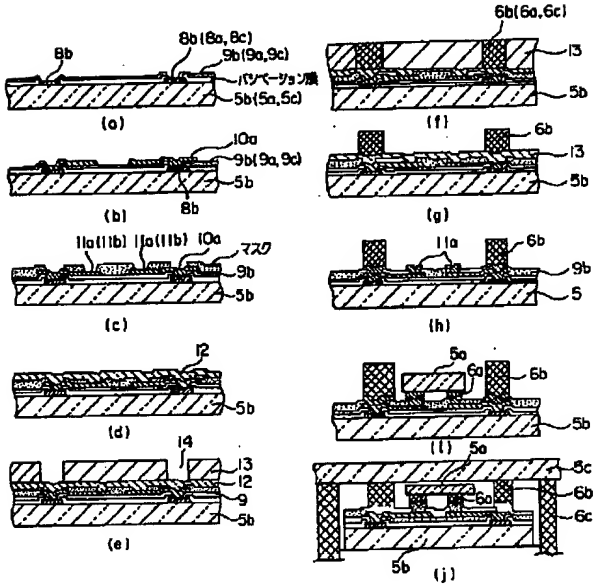
【手続補正書】
【提出日】平成５年１０月２０日
【手続補正１】
【補正対象書類名】図面
【補正対象項目名】全図
【補正方法】変更
【補正内容】

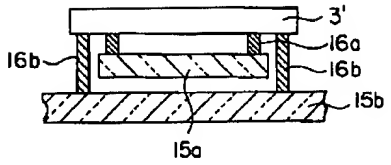
【図1】



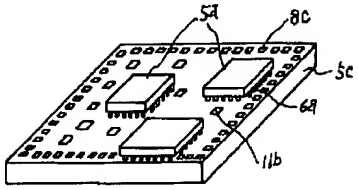

【図2】



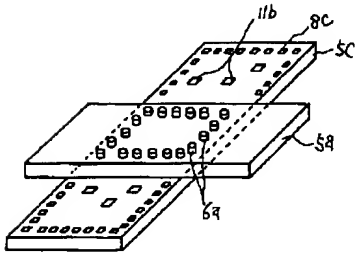

【図3】



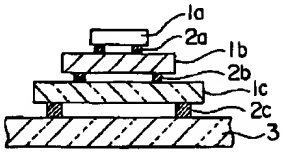

【図4】




【図5】




【図6】




【図7】